Winbond Electronics Corporation America
APPLICATION NOTE

## Initialization Procedures for WTS701 Text-to-speech Processor

1. Overview

The objective of this application note is to aid designers in integrating text-to-speech technology, specifically the WTS701, into new or exsisting designs. Crucial to any TTS design effort is the successful deployment of the chip's initialization procedures. This document describes the key initialization procedures for Winbond's WTS701 chip upon power up, and the SPI commands sent subsequent to power up.

1.1 Product Description

The WTS701 is the industry's first single chip text-to-speech processor that allows nearly instant addition of speech capability in a wide variety of applications. The WTS701 integrates a text processor, smoothing filter and multi-level memory storage array on to a single-chip. Text-to-speech conversion is achieved by processing the incoming text into a phonetic representation that is then mapped to a corpus of naturally spoken word parts. Figure 1 depicts a typical WTS701 configuration for an analog environment.

The WTS701 processor operates as a peripheral to a host controller, controlled by the system host via the SPI bus. This enables activation of speech functions through SPI commands, conversion of ASCII/Unicode text-to-speech, and driving the speaker directly. The WTS701 executes these commands and returns status information to the host controller.
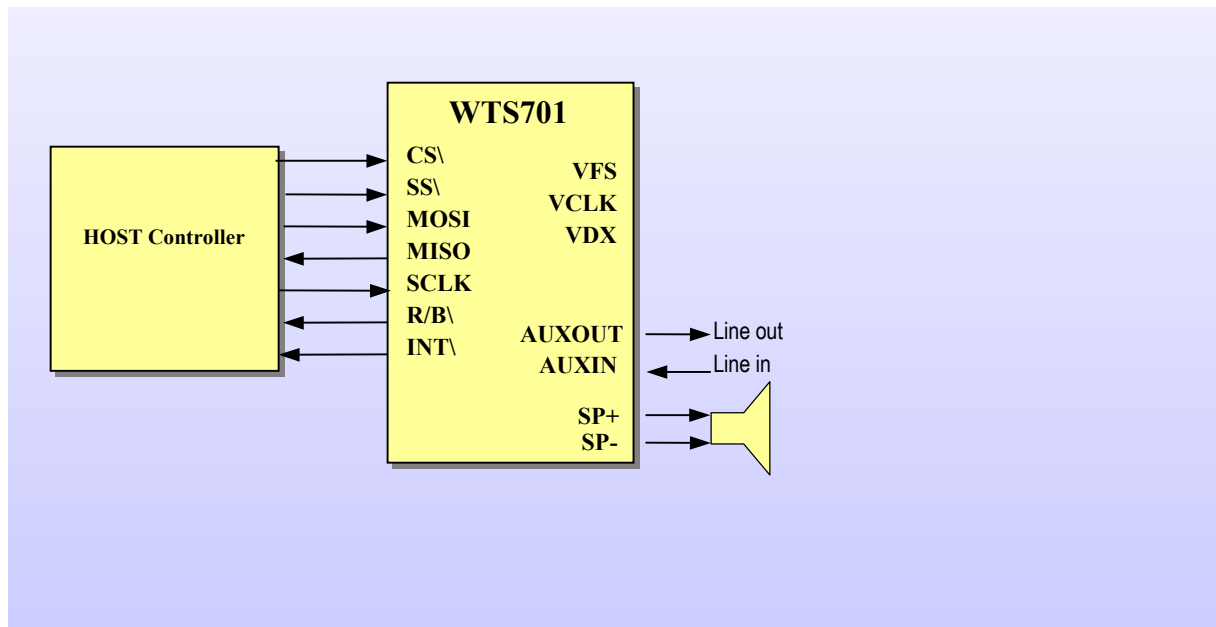

Figure 1. WTS701 Configuration for Analog Environment

2.1 Hardware Initialization

2.1.1 Powering Up the WTS701

To verify correct WTS701 device initialization, follow the steps outlined below:

1. Check that the Reset pin and the CS pin are grounded and not floating. Alternatively, if the host controller drives the Reset and CS pins, they should be set to LOW in the power up mode.

2. The WTS701 device has an internal power-on reset circuit that ensures correct initialization upon application of power. To activate POR, power needs to be applied to the WTS701 while Reset and CS pins are grounded and not floating. If the host controller drives the Reset and CS pins, they should be set to LOW during power up.

3. If you choose not to use the internal power-on reset circuit the WTS701 offers, the reset pin signal must be held HIGH for $0.5\mu s$ to achieve a reset and to put the WTS701 in the RESET state. Refer to Figure 2, which illustrates reset condition timing.

$$T_{reset}$$

$$T_{reset} > 0.5\mu s$$
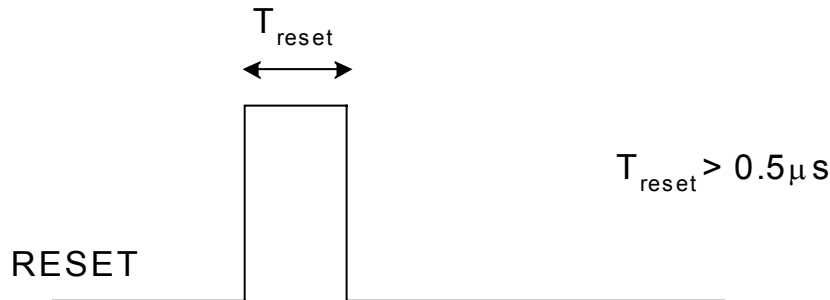
RESET

Figure 2. Reset Condition Timing

4. Once the WTS701 completes the reset, it will enter the POWER DOWN mode.

To recap, below is a summary of the steps that should be completed in order to power up the device:

1.   Apply power to Vcc
2.   Hold CS and RESET signals LOW
3.   The WTS701 goes to POWER DOWN mode when R/B\ pin or bit is asserted

2.1.2 Setting the WTS701 to IDLE state

Before issuing active commands, both clock configuration and device power up commands must be issued in the POWER DOWN mode. Upon successful transmission of these commands, the WTS701 will enter the IDLE state.

In general, commands can be sent only when R/B\ hardware signal or bit is asserted before every byte is sent. It is also required to verify that the command was accepted by validating ICMD bit value after a command was sent. For more information, please refer to application note, "Communicating With WTS701 Using SPI Bus" (publish date: December, 2002).

To recap, below is a summary of the steps that should be complted in order to place the WTS701 in IDLE state:

1. Send SCLC (Set Clock) command
2. Send PWUP (Power Up) command
3. Send RDST (Read Status) command, verifying processor ready to accept commands (RDY bit asserted)

The commands are further described on subsection 7.4.1, page 23 of the WTS701 datasheet (http://www.winbond-usa.com/products/tts/datasheets/index.shtml).

2.1.3 <u>Using Hardware RESET and Software RESET</u>

Once the WTS701 is in IDLE state, issuing a Reset command (RST) resets the WTS701 processor to the initial POWER DOWN state. In this case, the command sequence described in subsection 2.1.2 of this application note should be repeated.

Applying the reset pin by the host controller, while the chip is active, will reset the WTS701 to its default register values and the IDLE state. In this case, there is no need to re-send the commands that are described in subsection 2.1.2 of this document.

2.2 **WTS701 Operation Configuration**

As the WTS701 Text-to-Speech processor enters the IDLE state, it awaits commands sent to it to configure its operation. Note that the registers are set to default values and are to be modified whenever the application/system requires. Moreover, register values can be modified any time the WTS701 processor is in IDLE state to accommodate different real-time system configurations.
It is recommended that to verify that the proper value was accepted, the user should read a register value that was set using the RREG (Read Register) command.

To recap, below is a summary of the commands that could be sent to configure the WTS701 operation:

1. Send SCOM to set up communication register to enable interrupts
2. Send SCOD to set up CODEC configuration register
3. Send SAUD to set up audio control register
4. Send SVOL to set up audio control register
5. Send SSPD to set the initial speech output speed level
6. Send SPTC to set the initial speech pitch level

The configuration registers are described in greater detail in subsection 7.4.3, page 38 of the WTS701 datasheet http://www.winbond-usa.com/products/tts/datasheets/index.shtml).

3. <u>Sample Session</u>

After the initialization procedure, one can operate the WTS701 processor to set up the processor and perform text-to-speech conversion.

The following example describes SPI commands and their parameters in hexadecimal sent, as well as information received, to and from the WTS701 to initialize the processor and convert sample text to the speaker:

```
; Powering Up the WTS701
•   14 00   ; SCLC Set Clock command sent
    00 80   ; Status bytes received
•   02 00   ; PWUP Power Up command sent
    00 80   ; Status bytes received
            ; WTS701 enters IDLE state

; Verifying WTS701 is in IDLE mode
•   04 00   ; RDST Read Status command sent
    05 80   ; Status bytes received, WTS701 ready to accept commands (RDY bit asserted)
    00 00   ; Byte count received
•   12 00   ; RVER Read Version command sent (Optional)
    05 80   ; Status bytes received
    02 46   ; Hardware and Software version received (WTS701EM/T device)

; Setting WTS701 configuration registers (Optional)
•   4E 00   ; SCOM Set COM register command sent
    05 80   ; Status bytes received
•   4F 01   ; SCOD Set COD register command sent
    05 80   ; Status bytes received
•   50 43   ; SAUD Set AUD register command sent
    05 80   ; Status bytes received
•   51 03   ; SVOL Set VOL register command sent
    05 80   ; Status bytes received
•   52 02   ; SSPD Set speed command sent
    05 80   ; Status bytes received
•   77 05   ; SPTC Set Pitch command sent
    05 80   ; Status bytes received

; Verifying WTS701 VOL register value (Optional)
•   C0 51   ; RREG Read Register command sent
    05 80   ; Status bytes received
    00 03   ; VOL Register value received
```

; Sending text for conversion into speech
- 81 00 48 61 76 65 20 61 20 6E 69 63 65 20 64 61 79 1A
   ; CONV convert command sent with the text "Have a nice day"
   and following EOT character (0x1A Hex)
  05 80 05 80 05 80 05 80 05 80 05 80 05 80 05 80 05 80 ; Status bytes received
- 04 00   ; RDST Read Status command sent
  03 80   ; Status bytes received, converting, text buffer not empty
  00 00   ; Byte count received
- 04 00   ; RDST Read Status command sent
  87 80   ; Status bytes received, count interrupt occurred, converting, text buffer empty
  00 10   ; Byte count received
- 06 00   ; RINT Read Interrupt command sent to clear interrupts
  87 80   ; Status bytes received, count interrupt occurred, converting, text buffer empty
  00 10   ; Byte count received
- 04 00   ; RDST Read Status command sent
  07 80   ; Status bytes received, converting, text buffer empty
  00 12   ; Byte count received
- 04 00   ; RDST Read Status command sent
  85 80   ; Status bytes received, count interrupt occurred, text buffer empty
  00 12   ; Byte count received
- 06 00   ; RINT Read Interrupt command sent to clear interrupts
  85 80   ; Status bytes received, count interrupt occurred, text buffer empty
  00 12   ; Byte count received
- 04 00   ; RDST Read Status command sent
  05 80   ; Status bytes received
  00 12   ; Byte count received
- 04 00   ; RDST Read Status command sent
  25 80   ; Status bytes received, finished conversion interrupt occured
  00 12   ; Byte count received
- 06 00   ; RINT Read Interrupt command sent to clear interrupts
  25 80   ; Status bytes received, finished conversion interrupt occured
  00 12   ; Byte count received
- 04 00   ; RDST Read Status command sent
  05 80   ; Status bytes received
  00 12   ; Byte count received